01 / HOST GADGETEER J1 (SINGLE WIRING, MODE FROM CONFIGURATION) AND SERIES RESISTORS R1–R7

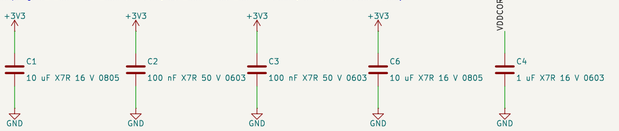


GADGETEER Y/U/S/I/P/A (config-selected)

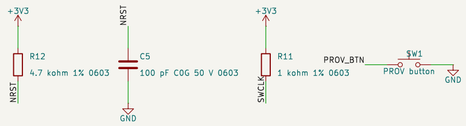
SJ1: 3V3 FEED, bridged by default, cut to measure or isolate



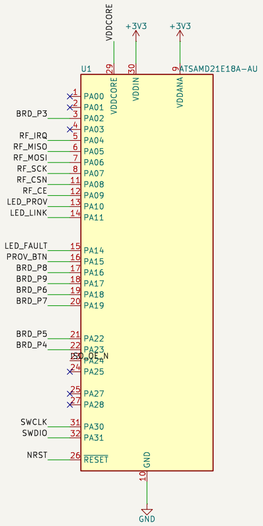
Decoupling: C1 10u + C2 100n at VDDIN, C3 100n + C6 10u at VDDANA, C4 1u at VDDCORE only



Reset / SWCLK / PROV button



02 / MCU U1 ATSAMD21E18A-AU (TQFP32), SUPPLY DECOUPLING, RESET, SWCLK PULL-UP



MODE TABLE (one wiring, mode set by the CRC-protected configuration record; contract gadgeteer_pin_map):

p3 PA02 (R1): GPIO (Y) / DAC out (A). p4 PA23 (R2): UART RX_IN (U) / GPIO. p5 PA22 (R3): UART TX_OUT (U) / GPIO.

p6 PA18 (R4): SPI CS_IN (S) / GPIO. p7 PA19 (R5): MOSI_IN (S) / PWM (P) / GPIO. p8 PA16 (R6): MISO_OUT (S) / SDA (I) / PWM (P).

p9 PA17 (R7): SCK_IN (S) / SCL (I) / PWM (P). J1 pin 2 (+5V) is not connected; pin 1 +3V3 enters through SJ1; pin 10 GND.

Radio SPI: SERCOM0 PA07 SCK, PA06 MOSI, PA05 MISO, PA04 IRQ (EXTINT4), PA08 CSN (GPIO), PA09 CE. SWD: PA30 SWCLK, PA31 SWDIO.

User interface: PA10 LED_PROV, PA11 LED_LINK, PA14 LED_FAULT (all active high), PA15 PROV_BTN (internal pull-up).

SAFE STATES: unpowered, reset, brownout (BOD33 about 2.8 V) and unconfigured: every host pin Hi-Z. Link lost > 100 ms: configured safe level, default Hi-Z with the configured pull; FAULT red latched; LINK green off. Provisioning: PROV amber on, UART TX Hi-Z until a valid frame.

No board output is energised by hardware alone. Mode mismatch is limited by R1–R7 (220 / 100 ohm) to about 9–13 mA per pin.

RF KEEP-OUT: module antenna end (about 4.3 mm) projects 5.0 mm past the board edge; no copper, vias, pour, screws or cable within 4 mm; no routing or components under the module body; B.Cu under the module is a GND pour only (Ebyte manual 4.1).

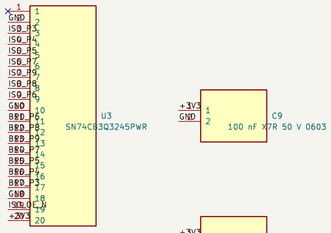
POWER BUDGET: +3V3 only, worst case 27.7 mA (radio 15.0 + MCU 7.5 + DAC 0.23 + 3 LEDs 5.0) against a 40 mA self-imposed budget, host allocation to this socket unknown (shared 0.32 A limit on the host). +5V: 0 mA. No hot-plug. Not for safety functions.

FIRST POWER: fit J2, SJ1 bridged, check TP1–TP2 = 3.3 V, then program over SWD (J2): hold SW1 at power-up to force provisioning.

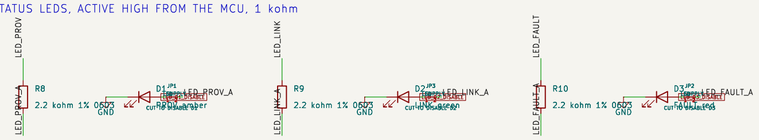
CAD-verified design intent only: first-article bench qualification required. v10 = study revision, CAD-clean UNQUALIFIED.

CERN-OHL-S-2.0 | KiCad only | black solder mask, white silkscreen | 2 layers 1.6 mm FR-4 | no ESD or backfeed protection (documented).

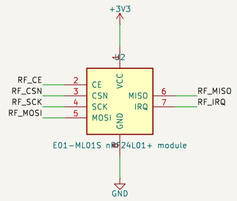




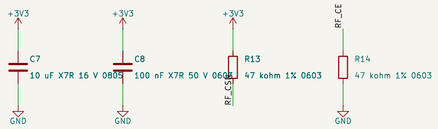
03 / STATUS LEDS, ACTIVE HIGH FROM THE MCU, 1 kohm



04 / RADIO MODULE U2 EBYTE E01-ML01S (ANTENNA END OVERHANGS THE BOARD EDGE), SUPPLY AND BIAS



C7 10u + C8 100n at module pad 1. R13 holds CSN high and R14 holds CE low while the MCU is in reset.





05 / SWD PROGRAMMING PADS J2 (NOT FITTED) AND TEST PADS (BOTTOM SIDE)





J2: 1 +3V3 (VTref), 2 SWDIO, 3 SWCLK, 4 NRST, 5 GND. Header not fitted. SWD is also the first-programming path.

v02 study revision: not qualified, not fabrication-ready
Wireless series master: Gadgeteer host side of an nRF24 remote-I/O link (SAM D21 + E01-ML01S)
Generated from design-contract.json by tools/create_schematic.py
Smoothieware / CERN-OHL-S-2.0

Sheet: /
File: wireless-series-master.kicad_sch

Title: Wireless series master (Gadgeteer side)

Size: A2	Date: 2026-10-01	**Rev: v10**
KiCad E.D.A. 9.0.8		Id: 1/1