PIN MAP (CLAUDE.md S row, both sockets: 1 +3V3, 2 +5V, 10 GND): J1 3 BUSY_H (out), 4 KILL_H (in), 5 CS_CHAIN_H, 6 CS_H, 7 MOSI_H, 8 MISO_H, 9 SCK_H.

J2 chain: 1 CH_3V3, 2 CH_5V, 3–5 not connected, 6 CH_CS (host pin 5, transformed), 7 CH_MOSI, 8 CH_MISO, 9 CH_SCK, 10 GND. Links JP6–JP11 closed (shipped).

U2 SN74AHCT125 (5 V): CS_H, SCK_H, MOSI_H –> *_5V, then 1 k series R2–R4 at the AVR end; gate 4 input GND, output open, OE high.

U3 SN74LVC125A (3.3 V): MISO_AVR –> MISO_H gated by CS_H (hi–Z while deselected), BUSY_AVR –> BUSY_H (OE GND), gates 3–4 parked.

Power: J7 5 V EXT –> F1 0.75 A PPTC –> Q1 P–MOSFET reverse block (D2 5.1 V gate zener, R16) –> +5V_EXT; D1 SMAJ6.0A clamp; JP1 1–2 EXT (shipped) / 2–3 HOST.

JP2 feeds +5V_LOGIC from the host +5V_H (closed). JP1 pads 1 and 3 are never bridged together. NO overvoltage cutoff: J7 is 5 V ONLY.

JP3 I2C pull–ups (closed). JP4/JP5 backlight polarity: shipped 1–2 bridged (LCD pin 15 = A via R17, pin 16 = K). Cut JP4 to disable the backlight.

ONE PANEL ONLY: J3, J4/J5 and J6 share LCD_*, ENCA, ENCB, CLICK, BEEP and +5V_PANEL. D3 = POWER 5V LOGIC, D4 = POWER 5V PANEL (a dark LED is not proof of safety).

Study v03: ERC clean, native opens/thermals remain: not fabrication–ready, not physically qualified, V2 host driver absent. CERN–OHL–S–2.0 | KiCad only | black mask, white silk.

Not fabrication–ready; CAD–checked design intent only; physical qualification and V2 host driver pend
v04 study: one LCD_RS repair and dense connector solid ground; 24 opens, unqualified
Retained circuit; v04 bounded endpoint routing repair
Smoothieware / CERN–OHL–S–2.0
Sheet: /
File: universal–panel–adapter.kicad_sch

Title: Smoothie universal panel adapter

Size: A0 | Date: 2026–10–11 | **Rev: v04 (study)**
KiCad E.D.A. 9.0.8 | Id: 1/1