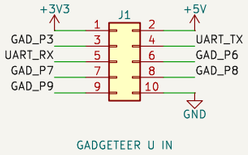
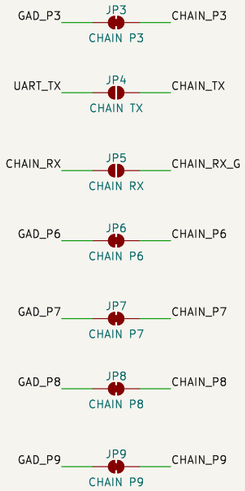
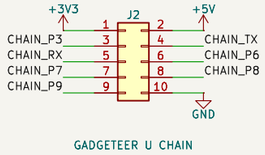
01 / GADGETEER U SOCKET J1 (IN), CHAIN LINKS JP3..JP9, CHAIN SOCKET J2









NOTES

Pin map (D1): U socket 1 +3V3, 2 +5V, 3 GPIO!, 4 TX (host out), 5 RX (host in), 6 GPIO, 7–9 [UN], 10 GND.

Direction labels are the SMOOTHIE viewpoint: header pin 4 RX IN receives cable TXD (orange), header pin 5 TX OUT feeds cable RXD (yellow).

J3 pins 2 and 6 (CTS#, RTS#) are not connected. J3 pin 3 (HDR_5V) is an OUTPUT of the FTDI cable: JP10 stays OPEN with an FTDI cable.

Chain defaults: JP3 JP6 JP7 JP8 JP9 bridged, JP4 (TX) JP5 (RX) JP10 OPEN. ONE UART TALKER: bridge JP5 on one board only.

D1 and D2 form a wired-AND on UART_RX with the single pull-up R3; D3 blocks cable VCC from the Gadgeteer +5V rail when JP10 is bridged.

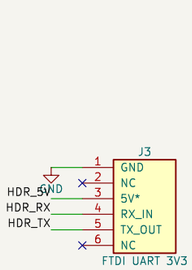
Logic is 3.3 V and the board is NOT 5 V tolerant (NO 5V LOGIC). No hot-plug claim. No pulse stretching on the activity LEDs.

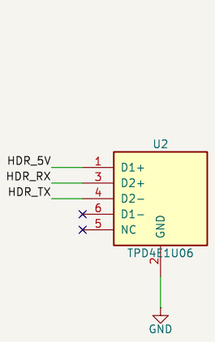
U1 inputs are plain taps on UART_TX / UART_RX, no series part. U2 pin 4 (D2−) is used as a channel; U2 pins 5 and 6 are no-connect.

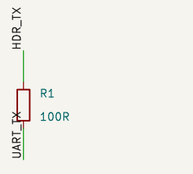
No external power input, so the 12–24 V 5V-source jumper rule does not apply.

CERN-OHL-S-2.0 | KiCad only | black solder mask, white silkscreen | v01 study, not for fabrication.

02 / FTDI HEADER J3, ESD U2, SERIES R1 R2, RECEIVE MERGE D1 D2 R3, OPTIONAL 5 V FEED JP10 D3

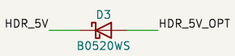






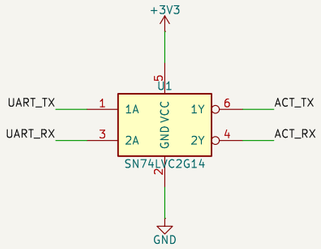


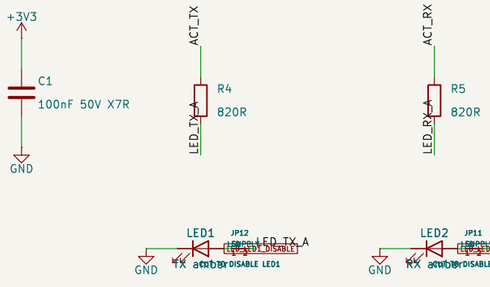




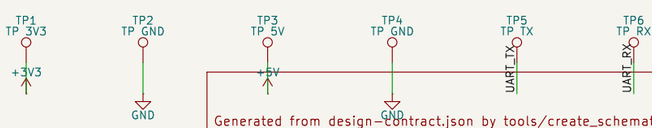


03 / ACTIVITY MONITOR U1 (HIGH-IMPEDANCE TAPS ON UART_TX / UART_RX), BYPASS C1, LEDS





04 / TEST POINTS (BOTTOM SIDE, OBSERVATION ONLY)



Generated from design_contract.json by tools/create_schematic.py
Gadgeteer U socket to FTDI TTL-232R header, 3.3 V logic, study version, not for fabrication
Smoothieware / CERN-OHL-S-2.0

Sheet: /
File: uart-breakout.kicad_sch

Title: Smoothie UART breakout (FTDI header, 3.3 V logic)

Size: A3	Date: 2026-10-01	**Rev: v10**
KiCad E.D.A. 9.0.8		Id: 1/1