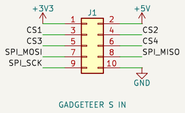
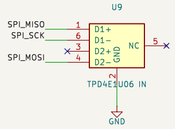
01 / HOST INPUT J1 (S), INPUT ESD CLAMP U9 AND MISO BIAS R29







PIN MAP (D1, CLAUDE.md S row, all five sockets: 1 +3V3, 2 +5V, 10 GND):

J1 IN: 3 CS1, 4 CS2, 5 CS3, 6 CS4, 7 MOSI, 8 MISO, 9 SCK. OUTn: 6 CSn (direct), 7 MOSI, 8 MISO, 9 SCK, 3–5 not connected.

Un = SN74CB3Q3125: 1A/1B SCK, 2A/2B MOSI, 3A/3B MISO, 1OE=2OE=3OE=CSn (switch closed while CSn is low), 4OE=+3V3 (channel 4 off, 4A=4B=GND).

Cell truth table: CSn low = port connected, LED on. CSn high or floating (Rn 10k pull-up) = port isolated, LED off. Hub unpowered = Ioff isolation.

SCK idle bias JPn (R3): pads 1–2 bridged = idle LOW via 100k (SPI modes 0/1, default); cut 1–2 and bridge 2–3 = idle HIGH (modes 2/3). MOSI idles low via 100k.

Signal order per output: connector pin – TVS U(4+n) – series R (33R SCK/MOSI, 100R MISO) – Un B pin. MISO host bias: R29 100k to +3V3.

D2 envelope: 3.3 V logic, SPI modes 0–3, SCK <= 10 MHz, cables <= 150 mm, one port selected at a time. Calculated, not bench verified.

D5: +3V3 and +5V pass straight from J1 to all outputs (shared, unswitched, no fuses): +5V is not used locally. Host 5 V regulator approx. 3 A shared.

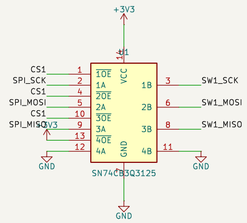
R10: not for active-high CS or 5 V devices (e.g. RRD ST7920 GLCD). The hub only stops a device on an unselected port from contending on the shared bus.

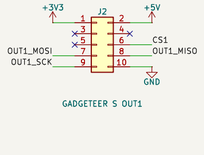
R9: outputs are fan-out endpoints, so the CLAUDE.md daisy-chain jumper rule is a documented deviation. No external power input: 12–24 V jumper rule N/A.

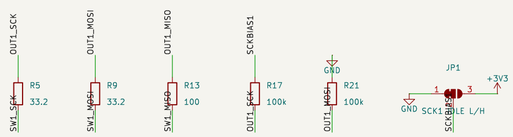
Open risk: research.md says V2 Prime headers may carry 5 V on pin 8 and 3.3 V on pin 9 (conflicts with canonical 1=3.3V, 2=5V); physical pin-1 marking not inspected.

CAD-verified design intent only; first-article bench qualification required. CERN-OHL-S-2.0 | KiCad only | black solder mask, white silkscreen.

02 / OUT1 CELL: U1 BUS SWITCH, ENABLED WHILE CS1 IS LOW

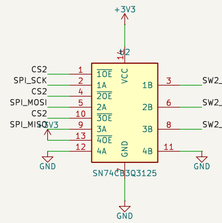


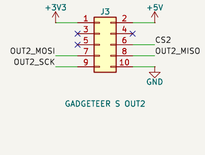


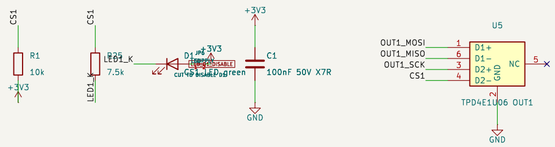


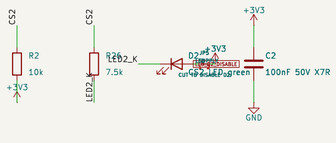


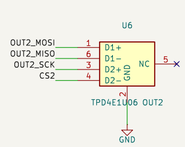
03 / OUT2 CELL: U2 BUS SWITCH, ENABLED WHILE CS2 IS LOW



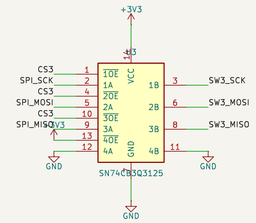


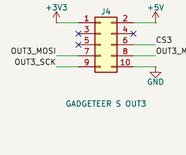


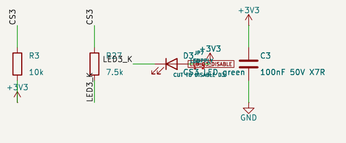


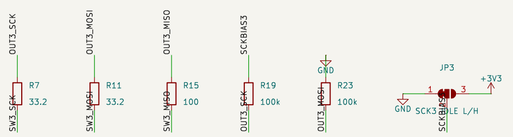


04 / OUT3 CELL: U3 BUS SWITCH, ENABLED WHILE CS3 IS LOW

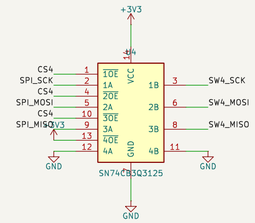


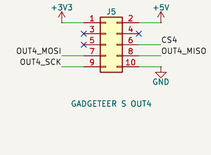


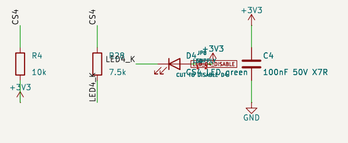


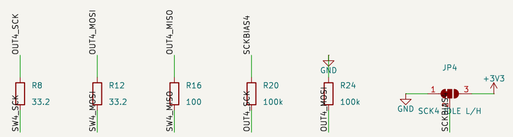


05 / OUT4 CELL: U4 BUS SWITCH, ENABLED WHILE CS4 IS LOW









SPI hub: one S input fans out to four S outputs through per-port quad bus switches
Generated from design_contract.json by tools/create_schematic.py
Smoothieware / CERN-OHL-S-2.0

Sheet: /	
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Size: A2	Date: 2026-09-26
KiCad E.D.A. 9.0.8	Id: 1/1

Rev: v10