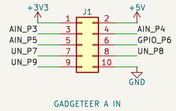
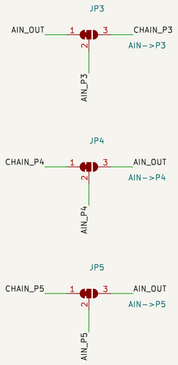
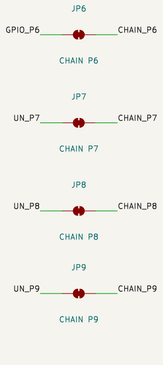
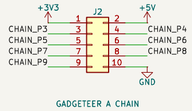
01 / GADGETEER A SOCKETS: J1 IN (HOST), SELECTOR JP3..JP5, CHAIN LINKS JP6..JP9, J2 CHAIN



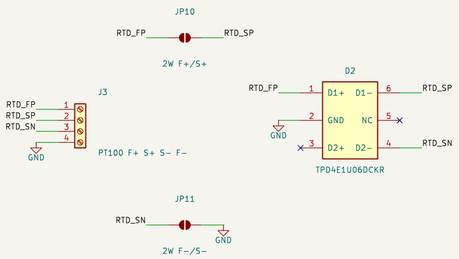




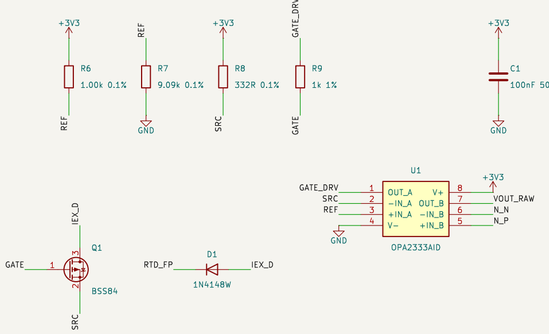




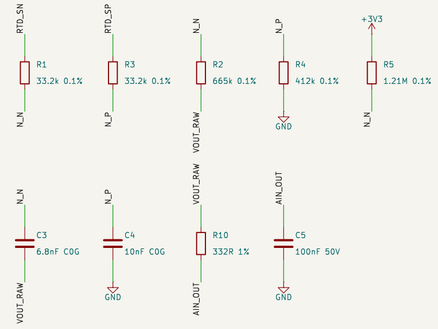
02 / PT100 TERMINAL J3 (F+ S+ S− F−), TVS D2, WIRE−MODE STRAPS JP10 JP11



03 / CONSTANT−CURRENT SOURCE U1A + Q1 + R8 (Iex 0.985 mA) AND U1 SUPPLY DECOUPLING



04 / DIFFERENCE STAGE U1B (R1..R5 C3 C4), OUTPUT R10 C5, TEST POINTS TP1..TP5





PIN MAP (D1, CLAUDE.md A row, J1 host / J2 chain): 1 +3V3, 2 +5V (not used locally, 0 mA), 3 AIN (GI), 4 AIN (G), 5 AIN, 6 GPIO, 7−9 [UN], 10 GND.

Chain defaults: JP3 1−2 bridged (AIN_OUT drives host pin 3, pin 3 not forwarded); JP4, JP5 1−2 bridged (pins 4, 5 forwarded: 2−3 hands the pin to AIN_OUT); JP6..JP9 bridged (cuttable).

Output−pin selector table: JP3 1−2 = OUT on pin 3 (default) / 2−3 = FWD; JP4 and JP5 1−2 = FWD (default) / 2−3 = OUT. Each chained board needs exactly one OUT pin, all different.

Wire modes: 4−wire = JP10 open, JP11 open (default). 3−wire (one−sided) = JP11 bridged only. 2−wire = JP10 and JP11 bridged. RTD_SN reaches GND only through JP11.

Terminal J3: 1 F+ (RTD_FP), 2 S+ (RTD_SP), 3 S− (RTD_SN), 4 F− (GND). PT100 ONLY, NOT K−TYPE. Wire with power off. No 12−24 V on the terminals.

Transfer (VCC 3.3 V, ratiometric x = Vout/VCC): 0 C 0.153 V (x 0.0464), 100 C 0.910 V, 200 C 1.645 V, 300 C 2.356 V, 400 C 3.045 V (x 0.9226). Iex = VCC R6/(R6+R7)/R8 = 0.985 mA.

Difference stage: Vout = Gd (Vs+ − Vs−) − Gz VCC with Gd = R2/R1 = 20.03 and Gz = R2/R5 = 0.550; R4 matches the + path gain to Gd within 0.3 %. C3 R2 and C4 R4 form matched 4.5 ms / 4.1 ms filters.

Protection: D2 (TPD4E1U06) on RTD_FP, RTD_SP, RTD_SN at the terminal; D1 blocks F+ back−feed into VCC through Q1; R1 R3 33.2k limit U1B input current. No clamp to +3V3.

Residual risk: a sustained 12−24 V on any terminal is not survived. Every single−wire open or short reads cold (output at the low rail): firmware min_temp must stay at 0 C or higher.

R1..R8 are Yageo RT thin film 0.1 % 25 ppm/C; R9 R10 are 1 % thick film. Single +3V3 supply for U1; +5V is only passed from J1 to J2 (TP4 observes it).

U1: OPA2333AID SOIC−8, pins 1−4 channel A (current source), pins 5−8 channel B (difference stage). Q1 BSS84: 1 gate, 2 source, 3 drain. D1 1N4148W: pad 1 cathode (RTD_FP), pad 2 anode.

Host rail budget: 1.36 mA typical / 1.5 mA max from +3V3, 0 mA from +5V; self−imposed 5 mA limit including downstream chained boards (ratiometric error).

No external power input, so the 12−24 V to Gadgeteer 5 V source−jumper rule does not apply. Change links with power off. No hot−plug.

TVS D2: channels are interchangeable ESD diodes (pins 1, 3, 4, 6): RTD_FP pin 1, RTD_SN pin 4, RTD_SP pin 6, pin 3 spare and pin 5 NC, so the rotation−90 footprint passes the Kelvin pair without a crossing.

v14 is a study: CAD intent only, not built, not tested, not qualified. CERN−OHL−S−2.0 | KICad only | black solder mask, white silkscreen.

CAD study only / not qualified
Kelvin4−wire / nominal0−400 C
Analogue PT100 / Gadgeteer A
Smoothieware / CERN−OHL−S−2.0
Sheet: /
File: simple−pt100−amp.kicad_sch

Title: Smoothie simple PT100 amplifier (analogue)

Size: A2	Date: 2026−10−11	**Rev: v14**
KiCad E.D.A. 9.0.8		Id: 1/1