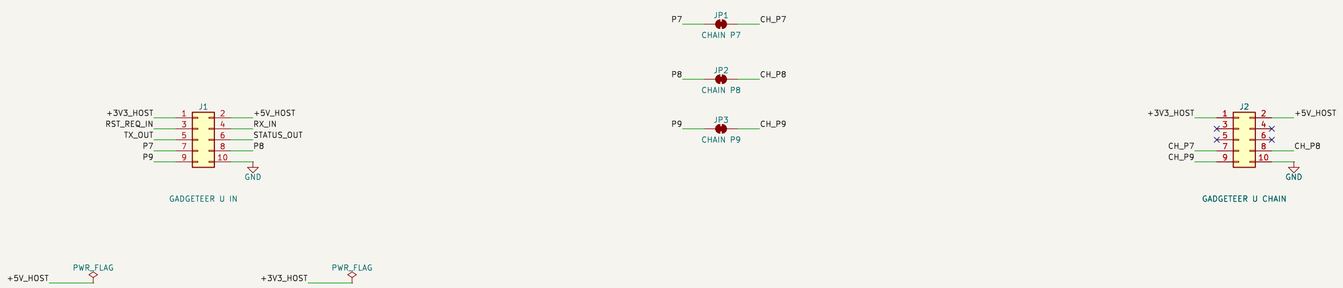
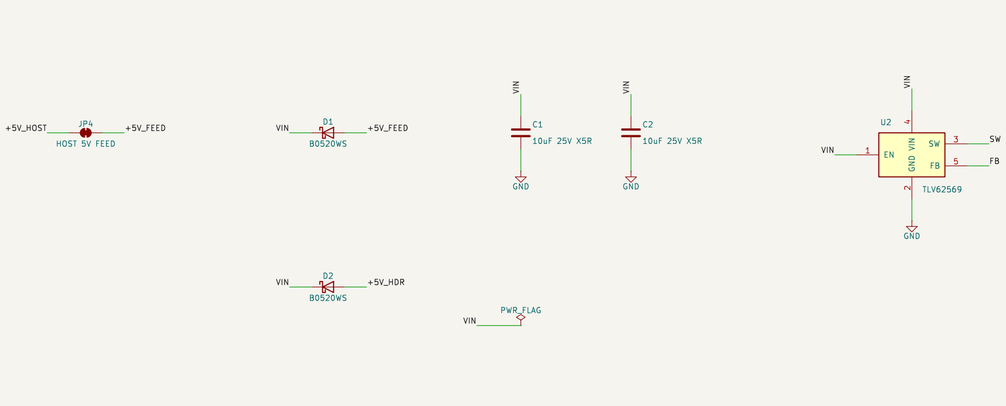
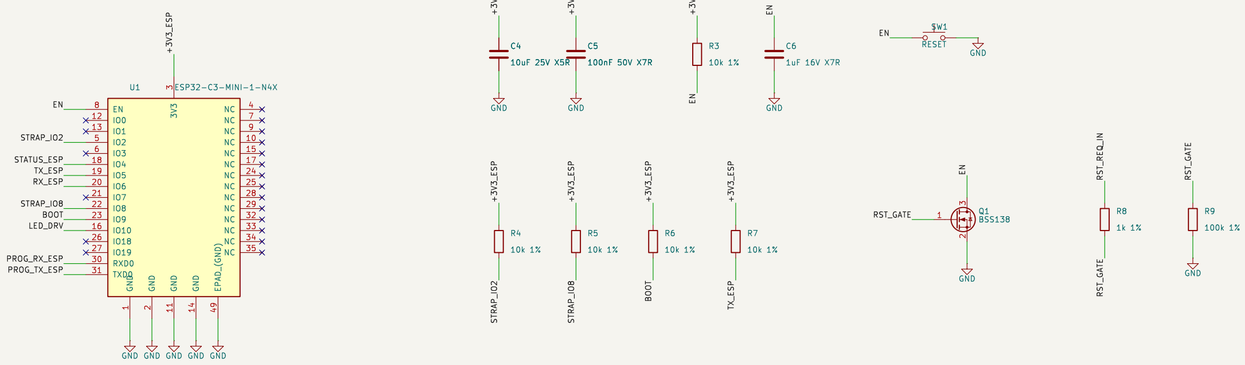
## 01 / GADGETEER U SOCKET J1 (IN), CHAIN LINKS JP1..JP3, CHAIN SOCKET J2



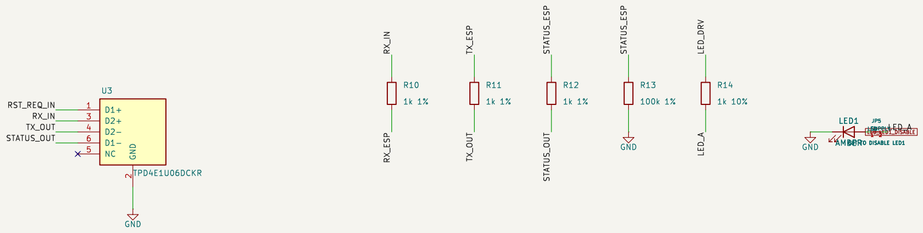

## 02 / POWER: HOST FEED LINK JP4, DIODE-OR D1 D2, BUCK U2 (5 V TO 3.318 V), L1, C1-C3, FEEDBACK R1 R2



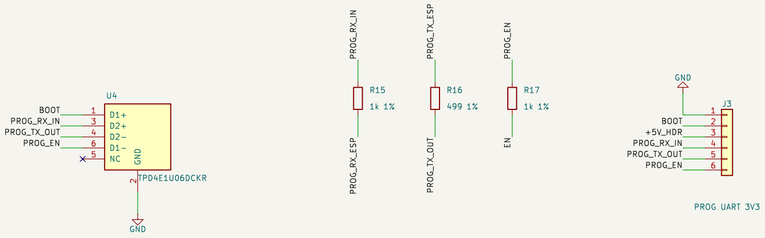

## 03 / MODULE U1, DECOUPLING C4 C5, STRAPS R4 R5 R6, TX PULL-UP R7, EN NETWORK R3 C6 SW1, RESET FET Q1 R8 R9



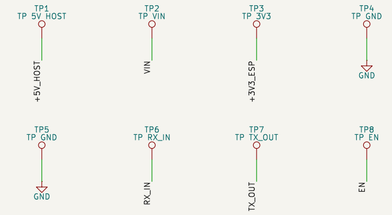

## 04 / HOST FRONT END: ESD U3, SERIES R10 R11 R12, STATUS PULL-DOWN R13, STATUS LED R14 LED1




## 05 / SERVICE HEADER J3 (UART0 + EN + BOOT), ESD U4, SERIES R15 R16 R17




## 06 / TEST POINTS (BOTTOM SIDE, OBSERVATION ONLY)




## NOTES

PIN MAP (D1): U socket 1 +3V3 (forwarded only), 2 +5V, 3 RST_REQ_IN (host asks for an ESP reset, HIGH = reset, floating = run), 4 RX_IN (host TX), 5 TX_OUT (host RX), 6 STATUS_OUT (low = not ready), 7-9 P7-P9 reserved, 10 GND.

Direction labels use THIS BOARD viewpoint (DR-003): RX_IN is ESP UART1 RX (IO6), TX_OUT is ESP UART1 TX (IO5, R7 10k pull-up keeps it idle-high while the ESP resets).

CHAIN: J2 pins 1, 2, 10 direct; pins 7-9 through cuttable jumpers JP1-JP3 (bridged by default); pins 3-6 NOT CONNECTED (consumed or driven here). JP4 is the HOST 5V FEED link (bridged by default), not a chain link: cutting it makes the host +5V supply nothing, power then comes from J3 pin 3.

POWER: only +5V is used. U2 TLV62569 buck, 5 V to 3.318 V (R1 453k / R2 100k, L1 2.2 uH, C3 10 uF). Host +3V3 is forwarded to J2 only and never used as a supply. D1 (host feed) and D2 (J3 pin 3) form a deliberate diode-OR. 5.5 V MAX. No 12-24 V input, so that jumper rule does not apply.

LOGIC is 3.3 V only (J3: 3V3 LOGIC ONLY). Powered plugging of the Gadgeteer cable and J3 is not claimed.

BOOT: IO9 is pulled up by R6 (SPI boot). A shunt on J3 pins 1-2 (BOOT to GND) plus a reset selects ROM download over UART0 (IO20/IO21 on J3 pins 5/4). EN is a wired-AND of R3 10k + C6 1 uF, SW1, Q1 and J3 pin 6 through R17.

GPIO PLAN: IO6 UART1 RX, IO5 UART1 TX, IO4 STATUS (R13 100k pull-down), IO10 LED1 via R14, IO2/IO8/IO9 strap pull-ups R4/R5/R6; IO0 IO1 IO3 IO7 IO18 IO19 unconnected (no-connect flags).

U1 symbol is authored locally from datasheet v2.2 table 3-1 (no stock ESP32-C3-MINI-1 symbol). GND pads 1 2 11 14 49 are visible; pads 36-48 and 50-53 are hidden power pins stacked on the pin 11 position, all on net GND.

PWR_FLAG sits on +5V_HOST, +3V3_HOST, +5V_HDR, VIN, +3V3_ESP and GND: these rails are fed through passive parts or by connectors and carry no power-output pin.

CERN-OHL-S-2.0 | KiCad only | black solder mask, white silkscreen | v01 study, not for fabrication.

QUALIFICATION: UART firmware, provisioning/authentication/update behavior, actual Smoothie host pinout and rail allocation remain unsigned.
ASSEMBLY/RF: module EPAD thermal-via paste/tenting process, antenna/enclosure clearance and regional finished-product conformity are unqualified.

Generated from design-contract.json by tools/create_schematic.py
Gadgeteer U socket to ESP32-C3-MINI-1 UART bridge, study version, not for fabrication
**Smoothieware / CERN-OHL-S-2.0**

Sheet: /
File: serial-to-wifi-board.kicad_sch

***Title: Serial to WiFi board (ESP32-C3 UART bridge)***

| Size: A2 | Date: 2026-10-11 | **Rev: v12** |
|---|---|---|
| KiCad E.D.A. 9.0.8 | | Id: 1/1 |