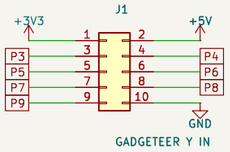
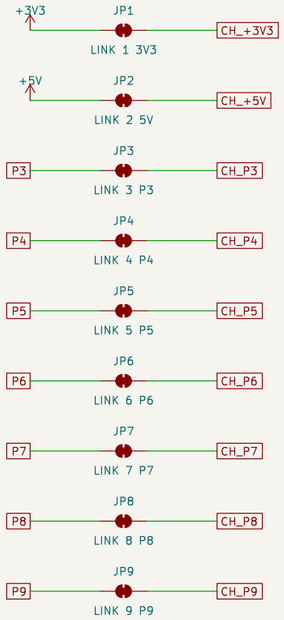
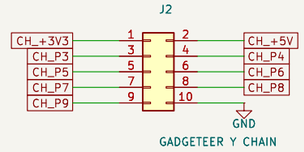
1 GADGETEER Y: HOST IN (J1) — NINE CUTTABLE CHAIN LINKS (JP1–JP9, SHIPPED BRIDGED) — CHAIN OUT (J2)



Y IN (host side). Odd pins left, even pins right, as the stock symbol draws a 2x5 header; pin k = Gadgeteer pin k.

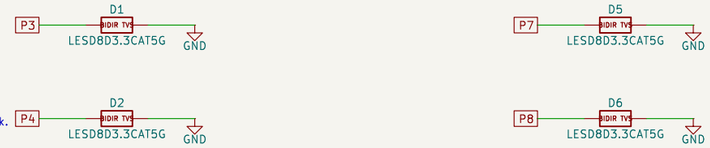


Pad 1 = IN side (host and terminal net). Pad 2 = CHAIN side (CH_ net). Cutting JPk opens only chain pin k.
GND (pin 10) has no link: it joins J1.10, J2.10, J3.10, TP1 and TP2 permanently.

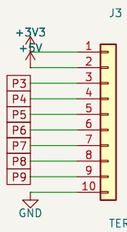


Y CHAIN (downstream). J2 pin k mirrors J1 pin k through link JPk; pin 10 (GND) is hard-wired.

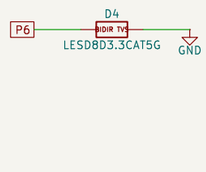
3 TERMINAL GPIO SHUNTS: CONDITIONAL 3V3 LOW-SPEED ONLY; HOST SURVIVAL UNQUALIFIED



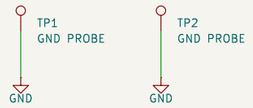
2 TEN 3.5 mm SCREW TERMINALS (J3): ONE POLE PER GADGEETER CONTACT, PIN k = TERMINAL k, TAPPED ON THE IN SIDE

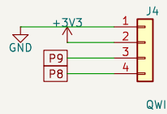


Terminal 1 = Gadgeteer pin 1 = 3V3 (HOST RAIL OUT, no external supply)
Terminal 2 = Gadgeteer pin 2 = 5V (HOST RAIL OUT, no external supply)
Terminal 3 = Gadgeteer pin 3 = P3 (raw 3.3 V logic GPIO)
Terminal 4 = Gadgeteer pin 4 = P4 (raw 3.3 V logic GPIO)
Terminal 5 = Gadgeteer pin 5 = P5 (raw 3.3 V logic GPIO)
Terminal 6 = Gadgeteer pin 6 = P6 (raw 3.3 V logic GPIO)
Terminal 7 = Gadgeteer pin 7 = P7 (raw 3.3 V logic GPIO)
Terminal 8 = Gadgeteer pin 8 = P8 (raw 3.3 V logic GPIO)
Terminal 9 = Gadgeteer pin 9 = P9 (raw 3.3 V logic GPIO)
Terminal 10 = Gadgeteer pin 10 = GND (return)



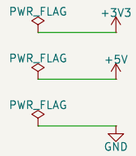
TP1 / TP2: top-side GND probe returns at the two ends of the terminal bank (observation only).





Qwiic: HOST I2C MODE ONLY. 1 GND; 2 3V3; 3 P9/SDA; 4 P8/SCL. No 5V, no second supply.

PWR_FLAGs: +3V3, +5V and GND are supplied by the host through J1; there is no regulator on this board.
+5V and +3V3 have no local load: they are passed to J3, to link JP1/JP2 and on to J2 (flags are deliberate).



NOTES

1. Pin map (CLAUDE.md section 3, Gadgeteer Y socket; host J32..J40 checked in the native Prime2590 files): pin 1 +3V3, pin 2 +5V, pins 3–9 raw GPIO P3–P9, pin 10 GND.

2. Passive adapter: no active parts, level shifting, series filtering, pull-ups, termination, LEDs or regulators. D1–D7 are passive bidirectional terminal-to-GND shunts; 3.3V standoff, low-speed loading and host survival require qualification. Every contact is forwarded unchanged to its terminal and, through link JPk, to J2.

3. Chain links JP1–JP9: shipped CLOSED (bridged solder jumpers, copper only). Cut only with host power off; restore factory state by re-bridging all nine with solder.

4. Current: no per-board allocation. The weakest element (SHF contact, ribbon, host header, shared ~3 A regulator, terminal) sets the limit; terminal pitch is not a power-rating upgrade. No numeric current rating is established; qualify host, cable, connectors and copper together.

5. Levels: P3–P9 are host 3.3 V logic. Do NOT apply 5 V to them. Rails 1 and 2 are host OUTPUTS: do not connect an external supply to them (back-feed). LOW VOLTAGE ONLY.

6. Verification boundary: CAD, ERC and netlist parity only. Host/cable mating, Samtec and Phoenix drawings, ratings, fabricator limits and enclosure fit are unverified.

7. Study version v17: unqualified, NOT FOR FABRICATION. CERN-OHL-S-2.0, KiCad only.

STUDY: unqualified, not for fabrication
Y Gadgeteer IN to ten 3.5 mm screw terminals, nine cuttable chain links, Y CHAIN
Smoothieware / CERN-OHL-S-2.0

Sheet: /
File: raw-pins-screw-terminal-breakout.kicad_sch

Title: Smoothie raw pins screw terminal breakout (Y)

Size: A3	Date: 2026-10-01	**Rev: v17**
KiCad E.D.A. 9.0.8		Id: 1/1