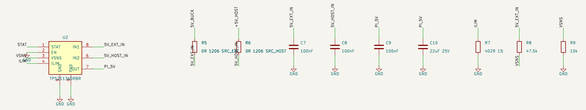
## 01 / EXTERNAL INPUT: J3 -> F1 FUSE -> D2 REVERSE BLOCK -> TVS D1 -> BUCK INPUT CAPS




## 02 / BUCK U1 LMR51430 (500 kHz PFM, 6.8 uH, 5.11 V OUT: EN divider R1/R2, FB divider R3/R4)




## 03 / SOURCE ARBITRATION U2 TPS2113A (IN1 = buck via R5, IN2 = host 5 V via R6, ILIM R7, VSNS R8/R9)




## 04 / UART PATH: J1 U SOCKET -> ESD D3 -> 100R -> LVC1G17 BUFFERS U3 / U4 -> J2 PI HEADER (TX/RX CROSS)




## 05 / STATUS LEDS (D4 5V POWER, D5 EXT SRC, D6 PI RXD, D7 PI TXD)




## 07 / TEST POINTS (BOTTOM, OBSERVATION ONLY)




PIN MAP (D1: CLAUDE.md s3 canonical socket U row): J1 pin 1 +3V3_HOST, 2 +5V_HOST, 3 GPIO? (NC), 4 TX = host transmit, 5 RX = host receive, 6 GPIO (NC), 7–9 UN (NC), 10 GND.

UART CROSSING (verified on the V2 Prime2660 netlist, J35.4 -> USART3_TX): J1.4 host TX -> D3 -> R12 100R -> U3 -> J2.10 (PI RXD0, GPIO15); J2.8 (PI TXD0, GPIO14) -> U4 -> R13 100R -> D3 -> J1.5 host RX.

U3 is powered from +3V3_PI, U4 from +3V3_HOST: the two 3V3 domains are never joined. R14/R15 100k keep the lines idle high; D6/D7 light while the line is low.

POWER PRIORITY (U2): OUT = IN1 (buck, via R5) while VSNS > 0.8 V (FB 47.5k / R9 10k from 5V_EXT_IN, priority above about 4.6 V), else the higher of IN1/IN2. U2.EN tied to GND (always enabled).

CURRENT LIMIT: ILIM = 500 / R7 = 500 / 402 = 1.24 A typ (0.95–1.55 A band), common to both sources; the board does not supply the 2.5 A the Pi brief recommends.

VARIANTS (R5/R6 0R 1206 links): A = both fitted (default); B = remove R6, external only; C = remove R5, host 5 V only (J3 unused). CLAUDE.md s4 12–24 V rule: R5/R6 = U2 select the 5 V source.

BUCK: LMR51430XDDCR 500 kHz PFM. FB R3 100k / R4 13.3k = 5.11 V nominal (set high on purpose to cover the U2 drop). EN divider R1 750k / R2 200k (rise 5.84 V, fall 5.23 V at the IC).

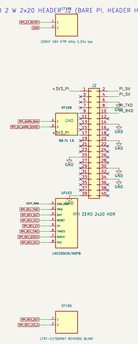
INPUT: J3 6.5–24 V DC (24 V SELV max, NO HOT-PLUG). F1 3 A. D2 B340A reverse block. D1 SMBJ24A TVS after D2 (clamp margin vs the 38 V abs max of U1 is thin, see questions.md Q-TVS).

WARNING: DO NOT POWER THE PI VIA USB while the host 5 V is present. U2 does not block current into +5V_HOST once IN2 is selected (questions.md Q-BACKFEED). PI 40-pin header unpopulated on the PI.

POWER FLAGS: GND, VEXT_RAW, +5V_HOST, +3V3_HOST, +3V3_PI (external supplies), plus VIN_BUCK, 5V_EXT_IN, 5V_HOST_IN (power_in pins of U1/U2 fed only through passive parts D2, R5, R6).

STATUS: STUDY, v01 first cut, NOT fabrication-ready. CAD-only: thermal, host-contact, PI stack fit and wireless checks are unverified. CERN-OHL-S-2.0 | KiCad only | black solder mask, white silkscreen.

## 06 / RASPBERRY PI ZERO 2 W 2x20 HEADER (BARE PI, HEADER HOLES UNPOPULATED)




## 08 / MECHANICAL: H1–H4 PI M2.5, H5–H6 PLATE M3, FID1–FID6 FIDUCIALS




No PI USB power with host. External 6.5–24 V DC.
Unqualified. Mux 1.24A A typical; 2.5 A target unmet.
**Smoothieware / CERN-OHL-S-2.0**

Sheet: /
File: rpi-zero-breakout.kicad_sch

**Title: RPi Zero 2 W UART carrier — STUDY**

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| Size: A0 | Date: 2026-10-11 | Rev: v12 |
| KiCad E.D.A. 9.0.8 | | Id: 1/1 |