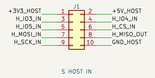
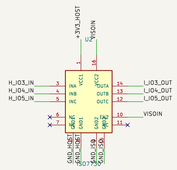
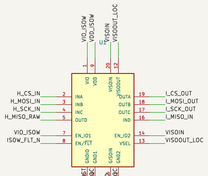
01 / HOST CONNECTOR J1 (S PROFILE, HOST SIDE)



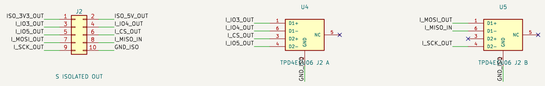
02 / ISO7730 U2: IO3, IO4, IO5 HOST TO PERIPHERAL



03 / ISOW7741 U1: CS, MOSI, SCK FORWARD, MISO REVERSE, ISOLATED DC–DC



04 / ISOLATED SPI S PORT J2 AND ESD ARRAYS U4 U5



S–ISO: ISOLATED SPI S PORT. Functional isolation <= 60 VDC between HOST and ISO domains; NOT a safety, mains or touch-voltage claim. UNSUITABLE FOR FABRICATION until reviewed and qualified.

PIN MAP (identical numbers on J1 and J2: rails 1 = 3V3, 2 = 5V, 10 = GND); 3 IO3, 4 IO4, 5 IO5, 6 CS, 7 MOSI, 8 MISO, 9 SCK.

Directions: pins 3,4,5,6,7,9 host to peripheral (U2 ch A–C = IO3–IO5; U1 ch A–C = CS, MOSI, SCK); pin 8 MISO peripheral to host (U1 ch D reverse, then U6 3-state).

J2 pins 1 and 2 are ISOLATED OUTPUTS (ISO_3V3_OUT from U3 LDO via JP3, ISO_5V_OUT from ISOW VISOOUT via FB4 and JP2), never forwarded host rails. J2 pin 10 = GND_ISO.

DOMAINS: HOST = +3V3_HOST +5V_HOST +5V_HOST_F VDD_ISOW VIO_ISOW GND_HOST GND1_LOC ISOW_FLT_N MISO_OE_N LED_HOST_A H_* nets. ISO = VISOOUT_LOC GND2_LOC ISO_5V ISO_5V_OUT ISO_3V3 ISO_3V3_OUT VISOIN GND_ISO LED_ISO_A I_* nets.

GND_HOST and GND_ISO are never connected: no bypass jumpers, no Y capacitor, no slot. U1 and U2 are the only parts with pads in both domains (8.1 mm HV land patterns).

JUMPERS (solder, shipped state): JP1 5V FEED bridged; JP2 5V OUT bridged; JP3 3V3 OUT bridged; JP4 LOGIC 3V3|5V pads 1–2 bridged = 3V3 logic (NEVER leave open); JP5 MISO pads 1–2 bridged = CS-gated, pads 2–3 = always driven.

Cut JP2 AND JP3 together if the peripheral is self-powered: its ground must go to J2 pin 10 only, JP4 pads 2–3 = 5 V logic for a 5 V peripheral that also drives MISO at 5 V.

POWER BUDGET: host +5V 0.15 A (U1 VDD 95 mA typ / 145 mA max at 45 mA isolated load, interpolated), host +3V3 20 mA, isolated load 45 mA of which peripheral 30 mA. Host header limiter about 0.32 A shared by ALL headers (not 3 A).

ISOW7741 layout: VSEL (pin 13) tied to VISOOUT (pin 12) for the 5 V mode; EN_IO1 = VIO, EN_IO2 = VISOIN (enabled); EN/FLT pulled to VIO by R1 10 k; C1 and C5 are 0402 within 1 mm of their pin pair; C3 and C7 bulk 22 uF.

SPI S profile: modes 0–3, 5 MHz target UNMET for tDO = 60 ns: 16.2 + 60 + 16.2 + 4.5 + assumed host setup 5 = 101.9 ns > 100 ns half-period, before cable/skew. No supported rate or ribbon limit qualified. Default output HIGH on supply loss; active-high IO3/IO4 enables go active on host loss.

ERC: PWR_FLAGs on +3V3_HOST +5V_HOST GND_HOST ISO_5V GND_ISO (contract) plus VDD_ISOW VIO_ISOW GND1_LOC GND2_LOC VISOIN (added: those power_in nets are fed only through ferrites or jumpers). No ERC downgrade or exclusion.

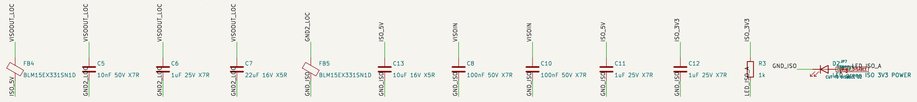
Verification boundary: CAD checks and calculations only; no measurement, isolation test, EMC result or safety certification. CERN-OHL-S-2.0 | KiCad only | black solder mask, white silkscreen.

PWR_FLAG placement (ERC drivers for passive-fed rails):

05 / HOST RAILS: FEED LINK, FERRITES, BYPASS, FAULT PULL-UP, LED



06 / ISOLATED RAILS: VISOOUT FILTER, LDO, LOGIC-LEVEL JUMPER, POWER OUTPUT LINKS, LED



07 / LDO U3, JUMPERS JP2 JP3 JP4, MISO 3-STATE BUFFER U6 AND CS GATE JP5



08 / TEST POINTS (OBSERVE ONLY): TP1–TP5 HOST, TP6–TP10 ISO, TP11–TP18 SPI PROBE PADS



STUDY / UNSUITABLE FOR FABRICATION: functional isolation only, no safety claim
Isolated SPI S pass-through: host S port to isolated S port, ISOW7741 + ISO7730 + MISO 3-state bu
Generated from design_contract.json by tools/create_schematic.py
Smoothieware / CERN-OHL-S-2.0
Sheet: /
File: opto-isolation.kicad_sch

Title: Opto-isolation pass-through board (S-ISO)

Size: A1	Date: 2026-10-11	**Rev: v12**
KiCad E.D.A. 9.0.8		Id: 1/1