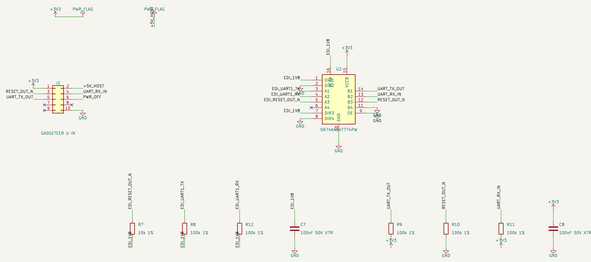
INTEL EDISON BREAKOUT v01 — REVIVAL PROTOTYPE — NOT FABRICATION-READY (study, footnote [bb] "edison is dead, ignore this one")

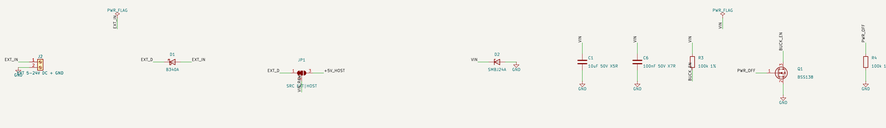
01 / HOST SOCKET J1 (Gadgeteer type U) AND 3-CHANNEL LEVEL TRANSLATOR U2 (module side 1.8 V left, host side 3.3 V right)

Pull-ups: R7 RESET_OUT_N (open drain), R8/R12 module UART idle bias; R9/R11 host UART idle bias, R10 pull-down. Decoupling C7 (1.8 V) and C8 (3.3 V) at U2.

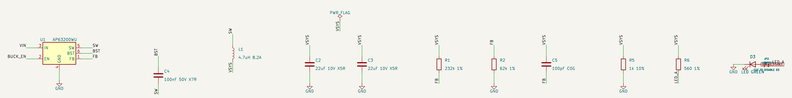


02 / EXTERNAL POWER INPUT J2 (5–24 V DC, NO HOT-PLUG) -> D1 -> JP1 (source select) -> F1 -> VIN. TVS D2. Input capacitors C1/C6, enable network R3/Q1/R4

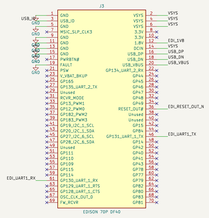
JP1 shipped bridged pads 1–2 = EXT (J2 through D1). Cut the strap and bridge 2–3 = HOST 5V from Gadgeteer pin 2 (bench option, about 0.3 A, never with J2 wired).



03 / BUCK CONVERTER U1 AP63200 (VIN 3.8–32 V in, VSYS = 0.8 V x (1 + R1/R2) = 0.8 x (1 + 232k/62k) = 3.794 V). Inductor L1, output C2/C3, bleeder R5, POWER LED D3



04 / MODULE CONNECTOR J3 (Hirose DF40C(2.0)-70DS-0.4V, Intel Table 5 pin names) AND USB MICRO-B J4 WITH ESD CLAMP U3





05 / TEST PADS (bottom side, observation only)



GADGETEER U SOCKET J1 (CLAUDE.md "Version 16"): 1 +3V3, 2 +5V_HOST (JP1 option only), 3 RESET_OUT_N (output to host), 4 UART_RX_N (host TX arrives), 5 UART_TX_OUT (board TX to host RX), 6 PWR_OFF (input, high = module power off), 7–9 not connected, 10 GND.

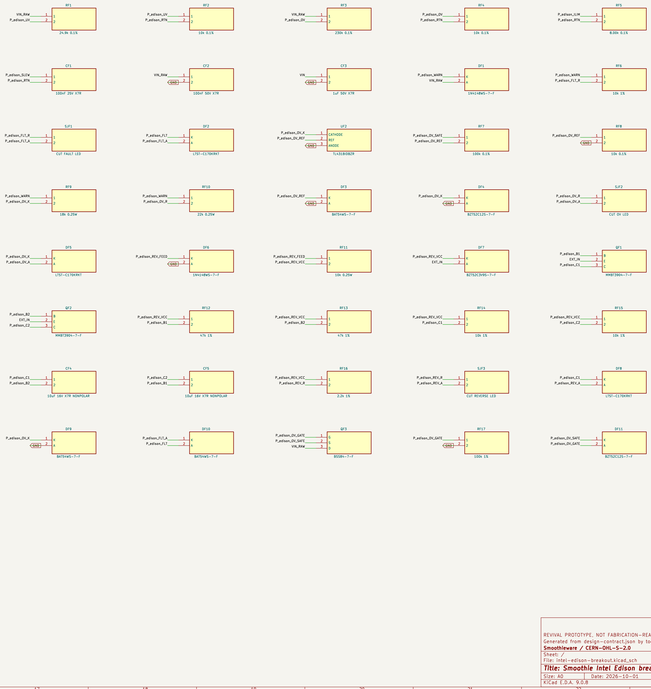
U2 CHANNELS: A1 EDI_UART1_TX -> B1 UART_TX_OUT (DIR1 = EDI_1V8); B2 UART_RX_N -> A2 EDI_UART1_RX (DIR2 = GND); A3 EDI_RESET_OUT_N -> B3 RESET_OUT_N (DIR3 = EDI_1V8); channel 4 unused (DIR4 = B4 = GND, A4 open); OE = GND; VCCA = EDI_1V8 (module pin 12), VCCB = +3V3 (host).

POWER: VSYS (3.794 V) feeds DF40 pins 2, 4, 6 and DCIN pin 14; module 1.8 V output (pin 12, max 100 mA) feeds only U2 VCCA and pull-ups; FAULT pin 19 and all six GND pads to GND; PWR_OFF high turns Q1 on and pulls EN low (cold power cycle). R4 keeps the input low when J1 pin 6 floats.

ASSUMPTIONS (design-contract.json open_assumptions): A05 module supply current 0.6 A continuous / 1.2 A peak is NOT from Intel (DF40 contact rating 0.9 A); A09 protection gaps (PPTC does not protect DF40 contacts, TVS clamp 38.9 V above PPTC Vmax 33 V, live 24 V connection may ring); A13 host 5 V allowance unknown (annotated 0.32 A limit on the Prime SYLIMIT rail versus the 3 A regulator remark).

USB: J4 micro-B -> U3 USBLC6-2SC6 (feed-through) -> module USB_DP/USB_DN pins 16/18; VBUS on pin 20 is a detect input only (the cable never powers the board); USB_ID pin 3 to J4 pin 4; shield and GND common.

CERN-OHL-S-2.0 | KiCad 9 only | black solder mask, white silkscreen | v12 STUDY: schematic and placement stage, not routed, not fabrication-ready.



REVIVAL PROTOTYPE, NOT FABRICATION-READY: Intel Edison carrier study
Generated from design-contract.json by tools/create_schematic.py
Smoothieware / CERN-OHL-S-2.0
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Title: Smoothie Intel Edison breakout (REVIVAL PROTOTYPE)

Size: A0 | Date: 2026-10-01 | Rev: v12
KiCad 10.0.X 10.0 | id: 1/1