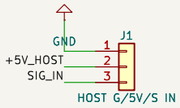
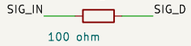
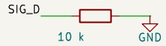
DSE-TX (EMITTER) — schematic, v10 CANDIDATE (physical qualification unsigned)

01 / HOST PORT J1: SIGNAL INPUT, ESD CLAMP, SERIES R AND PULL-DOWN







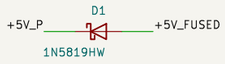






02 / HOST 5 V: PPTC, SCHOTTKY, DECOUPLING, CABLE-FEED LINK, LED, TEST PADS













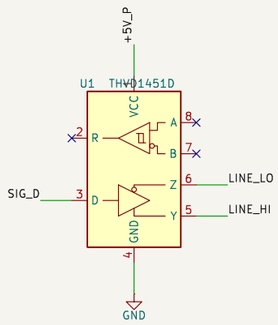








03 / DRIVER U1 (THVD1451D driver half only)



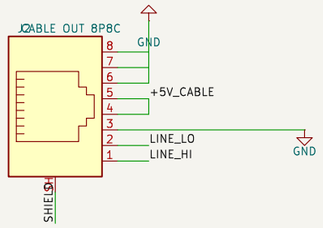
04 / CABLE JACK J2, CABLE-PIN TVS, SHIELD NETWORK











DSE v10 engineering successor. Native CAD evidence is separate from physical, host, cable and load qualification.

Cable: pins1/2 LINE_HI/LINE_LO; 3/6/7/8 GND; 4/5 +5V_CABLE. NOT ETHERNET / NOT PoE. No hotplug qualification.

RX: UCC27517 IN+ tied boost rail, IN- from fail-safe receiver R. Healthy idle R=HIGH gives SIG_OUT LOW; UVLO holds output LOW.

RX J1 pin2 remains +5V_R cable-derived OUTPUT. Boost powers signal driver only. Signal may exceed pin2: external load clamp/backfeed qualification REQUIRED.

NO CBL5V-OFF/local-feed variant: external RX supply is not authorized. Default cable feed only.

100 ohm / 10nF termination retained pending waveform decision: RC1us fails4x285ns and ideal68mA exceeds60mA recommendation.

25m/500kHz, 100mA output and old206.6ns latency are UNSIGNED targets; no empirical performance claim.

Single driver plus local boost on RX; native design review only

Smoothieware / CERN-OHL-S-2.0

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Title: DSE-TX v10 candidate

Size: A3	Date: 2026-10-11	**Rev: v10**
KiCad E.D.A. 9.0.8		Id: 1/1