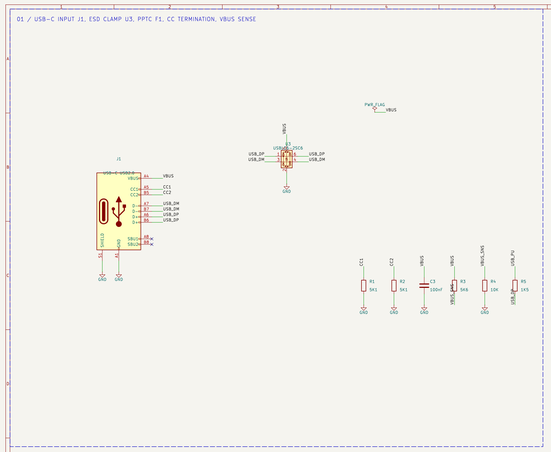
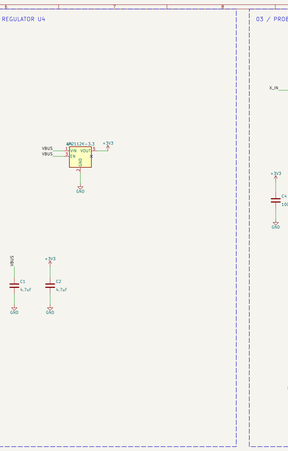
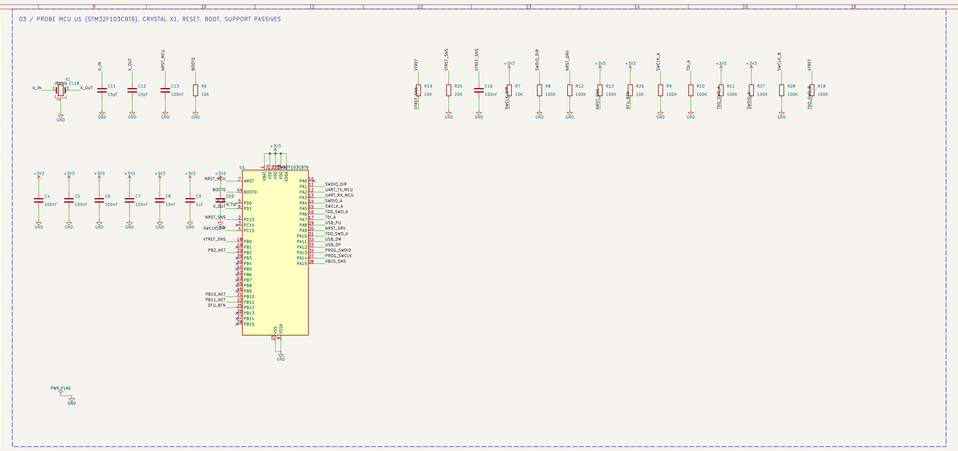
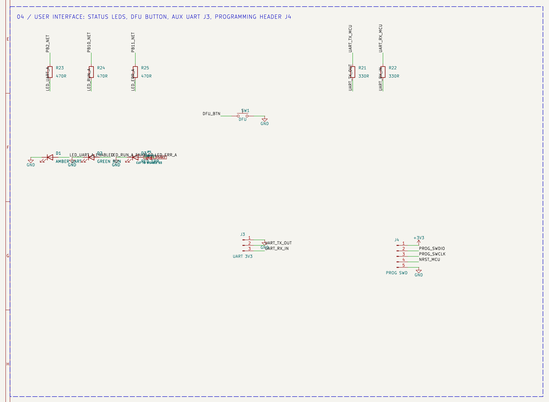
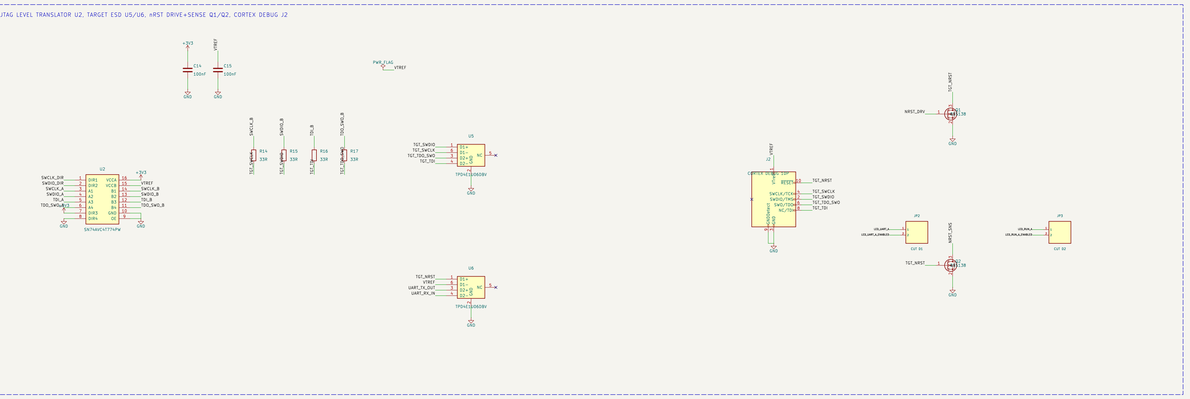
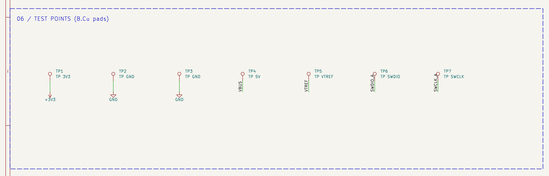












BMD NATIVE HW6 COMPATIBLE DEBUG PROBE, REV v12. HAZARD CLASS: LOW-VOLTAGE (USB 5 V IN, 3.3 V LOGIC, TARGET SIDE 1.65–3.6 V).

VTREF RANGE 1.65–3.6 V: SENSE AND TRANSLATOR REFERENCE ONLY, NO TARGET POWER (VTREF IS NEVER CONNECTED TO +3V3 OR VBUS). J2 IS NOT HOT-PLUG RATED.

FIRMWARE: BLACK MAGIC DEBUG NATIVE HARDWARE VERSION 6 (GPL-3.0, SEPARATE FROM THE CERN-OHL-S-2.0 HARDWARE). NO CLONE CLAIM. PIN MAP FROM PUBLIC platform.h.

PROVISIONING: (1) SWD PROGRAMMER ON J4 (PIN 1 IS A +3V3 SENSE, POWER FROM USB); (2) BMD BOOTLOADER AT 0x08002000, NATIVE APPLICATION AT 0x08002000;

(3) OPTION BYTE DATA1 = 0xFB06 (HARDWARE VERSION 6). UNPROVISIONED UNITS RUN AS HARDWARE VERSION 0: DO NOT CONNECT THEM TO A TARGET.

U2 FIXED DIRECTIONS: DIR1 = +3V3 (TDI A TO B), DIR2 = GND (TDO B TO A), OE = GND (ENABLED); PIN 15 VCCB = VTREF, PIN 16 VCCA = +3V3 MUST NEVER BE JOINED.

ERC NOTE: +3V3 HAS NO PWR_FLAG BECAUSE U4 VOUT IS A POWER OUTPUT; VBUS, VBUS_F, VTREF AND GND CARRY ONE PWR_FLAG EACH.

CALCULATIONS: 3V3 RAIL 72.3 mA WITH 20 PERCENT MARGIN (12 PERCENT OF LM); USB DRAW 72.7 mA; PA15 VBUS SENSE 2.86–3.38 V HIGH, << 0.35 V LOW; PB0 DIVIDER SCALE 0.9999.

VERIFICATION BOUNDARY: CAD CHECKS ONLY (ERC, NETLIST/PARITY, PLACEMENT SCRIPTS), NOT BENCH VERIFIED: USB ENUMERATION, SWD TIMING, SWO, BACK-FEED, ESD, THERMAL.

STUDY ONLY: FIRST-CUT CAD ATTEMPT, UNQUALIFIED. CERN-OHL-S-2.0 | KiCad only | black solder mask, white silkscreen.

PLATFORM PIN MAP (BMD native hardware version 6, sources/bmd-native-platform.h): signal | MCU pin | hardware

TMS / SWDIO | PA14 | SWDIO_A -> U2 A2 / B2 -> R15 -> TCT_SWDIO -> J2.2; R27 100 k pull-up on SWDIO_A

TMS_DIR | PA1 | SWDIO_DIR -> U2 DIR2, R8 100 k pull-down

TCK / SWCLK | PA5 | SWCLK_A -> U2 A1 / B1 -> R14 -> TCT_SWCLK -> J2.4; R9 pull-down on SWCLK_A, R28 pull-down on SWCLK_B

TCK_DIR | PC15 | SWCLK_DIR -> U2 DIR1, R7 10 k pull-up

TDI | PA7 | TDI_A -> U2 A3 / B3 -> R16 -> TCT_TDI -> J2.8

TDO / SWO (Manchester, TIM3 CH1) | PA6 | TDO_SWO_A <- U2 A4 / B4 <- R17 <- TCT_TDO_SWO <- J2.6

TRACESWO UART/NRZ (USART1 RX, 1wd) | PA10 | same net TDO_SWO_A

nRST drive | PA9 | NRST_DRV -> Q1 gate, R12 100 k pull-down; Q1 drain = TGT_NRST

nRST sense | PC13 | NRST_SNS = Q2 drain, R13 100 k pull-up; Q2 gate = TGT_NRST

TPWR sense (target voltage) | PB0 | VTREF_SNS = R19/R20 divider of VTREF, C16

PWR_BR / TRST (target power switch) | PB1 | not connected (no target power switch; DD)

USB_PU | PA8 | USB_PU -> R5 1.5 k -> USB_DP

USB D– / D+ | PA11 / PA12 | USB_DM / USB_DP via U3 ESD from J1

USB_VBUSS sense (1wd+) | PA15 | VBUS_SNS = R3/R4 divider of VBUS (5.6 k / 10 k)

LED_R UART | PB2 | R23 -> D1 amber

LED_G IDLE_RUN | PB10 | R24 -> D2 green

LED_B ERROR | PB11 | R25 -> D3 red

BTN1 / DFU request | PB12 | DFU_BTN: SW1 to GND, R26 10 k pull-up

UART TX (USART2 1wd) | PA2 | UART_TX_MCU -> R21 330 -> UART_TX_OUT -> J3.2; U6

UART RX (USART2 1wd) | PA3 | UART_RX_IN -> R22 330 -> UART_RX_MCU

OTG flash / AUX SPI / SD / display / VBAT (1wd+ options) | PB5–PB9, PB13–PB15, PA0 | not fitted, pins unconnected

hardware version | option byte Data1 | 0xFB06 programmed at provisioning (low byte 0x06, high byte its complement)

USB-C powered BMD native hw6 compatible SWD/JTAG probe; STUDY, unqualified
Generated from design-contraction by tools/create_schematic.py
SmoothHeart / CERN-OHL-S-2.0
Sheet: /
File: debug-probe.kicad_sch

Title: Smoothie debug probe (BMD native hw6 compatible)

Size: A0 | Date: 2026-10-08 | Rev: v12
KiCad E.D.A. 9.0.8 | Id: 1/1