HOST SIDE (Gadgeteer 3.3 V, GND_HOST)

ISOLATION BARRIER (U1)

LOAD SIDE — FLOATING GATE-DRIVE DOMAIN AND UNQUALIFIED LOAD SWITCH (SW_A / SW_B)

J1
SHF-105-01-L-D-TH-LC
GND_HOST
+3V3_HOST
EN_CMD

EN_CMD
R1
100R
EN_TPS
R2
10k
PXYR
R3
9.09k 1%
U1
TPSI3050DWZR
EN_TPS
PXYR
+3V3_HOST
GND_HOST
EN
PXYR
VDDP
VSSP
VDDH
VSSH
VDDW
VDDH
VSSW
SW_COM
EN_CMD
R9
2.2k
GND_HOST
LED1
green CMD
LED_A_ENABLED
TP1
+3V3_HOST
TP2
GND_HOST
TP3
EN_CMD
+3V3_HOST
C3
1uF 16V X7R
GND_HOST
+3V3_HOST
C4
100nF 16V X7R
GND_HOST
VDDH
R4
10R
VDDW
R5
10R
G1
R6
100k
SW_AF
G2
R7
100k
SW_B
SW_A
SW_B
D1
DT-SS-3P01-02
JP1
VIN_A
VIN_A_PWRCH
CUT JUDI
SW_AF
G1
Q1
CSD18536KTT
SW_COM
SW_B
G2
Q2
CSD18536KTT
SW_COM
VDDH
C1
2.2uF 16V X7R
SW_COM
VDDW
C2
2.2uF 16V X7R
SW_AF
D2
SMDJ33CA
SW_B
SW_A
F1
Keystone 3568 + ATM 30 A 32 V
SW_AF
PWR_FLAG
PWR_FLAG
PWR_FLAG
TP
VDDH
TP
SW_COM

STUDY v14 — NOT FOR FABRICATION — UNSUITABLE UNTIL HUMAN REVIEW. High-current hazard class (SELV DC 0–30 V, 32 V abs, 20 A design target with insulated heat sink). CAD/calculation only, no bench test.

Function: Isolated two-terminal DC solid-state switch. EN (J1 pin 3, 3.3 V, active high, Gadgeteer type X) -> R1 100R -> U1 TPSI3050 EN (R2 10k pull-down = default OFF) -> floating 10 V gate supply -> Q1/Q2 common-source series pair between SW_A and SW_B.

J1 = Gadgeteer socket type X: pin 1 +3V3_HOST (U1 VDDP), pin 2 +5 V NOT USED (no-connect), pin 3 EN, pins 4–9 no-connect (pin 4 reserved FAULT_OUT, not fitted), pin 10 GND_HOST.

ISOLATION: U1 is the only part crossing the HOST/LOAD barrier (pads 1–4 HOST, pads 5–8 LOAD, 9.1 mm pad gap). GND_HOST is NEVER joined to SW_COM. FUNCTIONAL isolation only — no safety claim, not for mains.

SW_A and SW_B are interchangeable (no polarity). F1 30 A ATM 32 V in series on the SW_A side; wire/overload protection only, NOT FET protection. D1 SMDJ33CA bidirectional TVS across SW_AF — SW_B clamps wiring-inductance energy only.

Inductive loads need an EXTERNAL freewheel diode across the load. External branch protection >= 25 A (12 rating 24–4 EC / 25 A UL; sibling data). OFF IS NOT ISOLATED: off-leakage unqualified, hot-pluggable.

U1 settings: three-wire standard enable. R3 9.09k on PXYR (TableB-1:26.75; worked example21.15); unresolved). C3 1uF + C4 100nF on VDDP. C1 = C2 = 2.2uF 16V X7R (CDV1/CDV2). gate resistors R4 = R5 = 10R, gate-source pull-downs R6 = R7 = 100k. LED1 shows EN pin high, NOT load state.

Pin types: U1 and Q1/Q2 use deliberate electrical pin types (no passive shortcut), so ERC checks power_in/output consistency for them: stock Device/Connector symbols are passive by KiCad convention.

PWR_FLAGs: +3V3_HOST and GND_HOST (supplied through the Gadgeteer cable), SW_COM (floating common-source node, the supply of U1 VSSS is the gate-drive return, no connection to any external rail). No flag on SW_AF; no power_in pin sits on it.

CERN-OHL-S-2.0 | KiCad only | black solder mask, white silkscreen | 2-layer 70 um (2 oz) copper.

STUDY v14 — NOT FOR FABRICATION — high-current hazard — unsuitable until human review
Generated from design-contract.json by tools/create_schematic.py
Smoothievent / CERN-OHL-S-2.0
Sheet: /
File: dc-ssr-board.kicad_sch
Title: Smoothie DC SSR board (study)
Size: A2 | Date: 2026-11-01 | **Rev: v14**
KiCad 8.0.4 | Id: 1/1