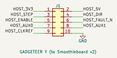
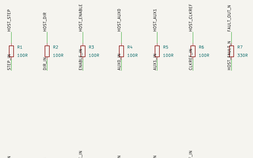
## 01 / HOST INPUT: J1 GADGETEER Y, 100R SERIES, 10k PULL-DOWNS, OR POWER LINKS R33 R34, TEST PADS

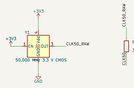


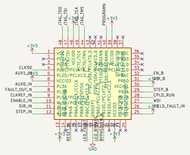



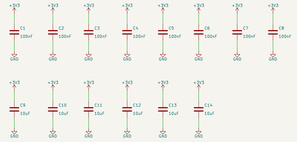




## 02 / CPLD: U1 LCMXO2-640HC QFN48, 50 MHZ CLOCK Y1, DECOUPLING C1–C14



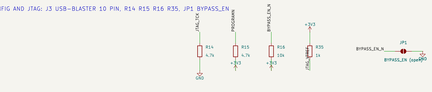



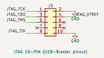





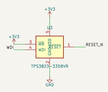


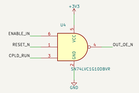
## 03 / CONFIG AND JTAG: J3 USB-BLASTER 10 PIN, R14 R15 R16 R35, JP1 BYPASS_EN




## 04 / HARDWARE PERMIT AND SUPERVISOR: U3 TPS3823, U4 NAND3 (OUT_OE_N), R17 R18 R19



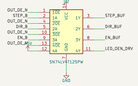










## 05 / OUTPUT 5 V: U2 SN74LV4T125 3-STATE BUFFER, 330R SERIES R21–R23, IDLE BIAS R24–R26










## 06 / FIELD I/O: J2 KK 1x6, U6 ESD ARRAY, FAULT RETURN R27 R28 U5
















## 07 / INDICATORS D1–D4 AND MOUNTING HOLES H1–H4







PIN MAP (IS, CLAUDE.md rev 1): J1 1 +3V3, 2 +5V, 3 STEP_IN, 4 DIR_IN, 5 ENABLE_IN (active high = motion requested), 6 FAULT_OUT_N (board to host, active low), 7 AUX6, 8 AUX7, 9 CLKREF, 10 GND.

J2 (D7, view from top, pin 1 west): 1 GND, 2 STEP_OUT, 3 DIR_OUT, 4 ENABLE_OUT_N (low = driver enabled), 5 FAULT_IN_N (low = fault), 6 GND. 5 V LOGIC ONLY, NO 12–24 V. NO HOT-PLUG.

SAFE STATE (DS): OUT_OE_N = NAND(RESET_N, CPLD_RUN, ENABLE_IN) drives all four OE pins of U2. R18 pulls OUT_OE_N to +5V; R17 CPLD_RUN, R10 ENABLE_IN, R19 WDI pull down. No CPLD pin touches OUT_OE_N. U2 outputs, J2 or U6.

IDLE BIAS (variant A, active-low driver enable): R24 R25 pull STEP_OUT DIR_OUT to GND; R26 pulls ENABLE_OUT_N to +5V. Loss of the board +5V with +3V3 present leaves ENABLE_OUT_N at 0 V: documented limitation, gate Q07.

POWER: HOST_3V3 and HOST_5V enter through removable 0R links R33 and R34; JP1 ships OPEN. No second Gadgeteer socket, no pass-through (D10). No external power input.

U1 pins 2 3 14 18 17 21 23 24–38 41–43 are left unconnected on purpose (spare/JTAG/config dual-function pins DONE INITB JTAGEN SDA SCL CSSPI0 MCLK SO SN SI) also unused: SN and PROGRAMN must not be driven low).

Local symbols (deviation from schematic_rules.symbols): U1 LCMXO2-640HC-vSG48; U2 SN74LV4T125PW (stock symbol is derived and multi-unit); U3 TPS3823-33; U6 PESD5V0U1D.

Unverified: USB-Blaster pinout of J3, DRV8825 timing, host pin limits and cable orientation (questions.md, contract open_assumptions). STUDY ONLY: UNSUITABLE FOR FABRICATION until human review.

CERN-OHL-S-2.0 | KiCad only | black solder mask, white silkscreen | CPLD ADAPTER v11 VAR A

STUDY: unsuitable for fabrication until human review.
Single-axis STEP/DIR/ENABLE conditioner: Gadgeteer Y (3.3 V) to 5 V stepper driver logic via MachX
Generated from design-contract.json by tools/create_schematic.py
**Smoothieware / CERN-OHL-S-2.0**

File: cpld-adapter.kicad_sch

**Title: CPLD adapter**

| | |
|---|---|
| Size: A2 | Date: 2026-10-03 |
| KiCad 10.0.1 | Rev: v11 |
| | ID: 1/1 |