00 / PWR_FLAG supply markers (ERC only, no part)

PWR_FLAG
GND

PWR_FLAG
VIN_PROT

PWR_FLAG
BUCK_5V

PWR_FLAG
CHIP_3V

PWR_FLAG
HOST_3V3

PWR_FLAG
HOST_5V

PWR_FLAG
CHIP_3V3

PWR_FLAG
VEXT_IN

PWR_FLAG
HOST_5V_D

01 / POWER IN J2 EXT 7–24 V DC -> F1 -> D1 -> VIN_PROT

VEXT_IN
J2
EXT = 7–24V DC / -
GND

VIN_FUSED
D1
B340A

VIN_PROT
C7
47uF 35V Al-elec

VIN_PROT
D2
SMBJ33A

F1: PPTC Hold, 5V reverse block secured. D2 TVS and C7 behind D1 (only F1 sees a reversed source).

02 / BUCK U1 LMR51430Y 1.1 MHz VIN_PROT -> BUCK_5V 4.98 V

VIN_PROT
U1
LMR51430YDDCR
EN
FB
SW
BOOT
VIN
GND
GND

L1
3.3uH SRP5030CA-3R3M
SW
BUCK_5V

BUCK_5V
C5
22uF 16V X7R
GND

BUCK_5V
C6
22uF 16V X7R
GND

BUCK_5V
R1
100k 1%
FB
GND

FB
R2
13.7k 1%
GND

VIN_PROT
R3
715k 1%
EN

EN
R4
200k 1%
GND

BOOT
100nF 50V X7R
SW

VIN_PROT
C1
4.7uF 50V X7R
GND

VIN_PROT
C2
4.7uF 50V X7R
GND

VIN_PROT
C3
100nF 50V X7R
GND

CL/CX ≈7 uF < C3 100 nF < VIN bypass. CX/CX = 2 + 22 uF out. R1/R2 FB divider 100k/13.7k (4.98 V). R3/R4 EN UVLO 715k/200k (rise 5.8 V typ).

03 / SOURCE SELECT SJ1 EXT | HOST -> CHIP_5V (CHG-IN)

BUCK_5V
SJ1
HOST_5V_D
PWR SRC: EXT | HOST
HOST_5V

D4
PMEG3050EH
HOST_5V_D

CHIP_5V
R11
1k
CHIP_5V

CHIP_5V
D3
SMS10A
GND

CHIP_5V
C4
10uF 10V X5R
GND

SJ1: stripped Bridge(2) = EXT. HOST position (2–3) via 0k << 0.3 A, unsupported above. D3 SMBJ5.0A clamps CHG-IN.

04 / UART BRIDGE J1 (U) host 3.3 V <-> CHIP UART1 3.3 V, gated buffers

HOST_3V3
J1
GADGETEER U IN
HOST_3V3
HOST_TX_IN
HOST_5V
HOST_TX_IN
GND

HOST_3V3
HOST_TX_IN
U2
SN74LVC1G126DBVR
CHIP_RX_OUT
CHIP_3V3
GND
SN74LVC1G126DBVR host->CHIP

CHIP_3V3
CHIP_TX_IN
U3
SN74LVC1G126DBVR
HOST_RX_OUT
HOST_3V3
GND
SN74LVC1G126DBVR CHIP->host

CHIP_3V3
C8
100nF 16V X7R
GND

HOST_3V3
C9
100nF 16V X7R
GND

HOST_TX_IN
R5
100k 1%
LED_TX5_A

CHIP_RX_OUT
R6
10k 1%
CHIP_RX_OUT

CHIP_TX_IN
R7
100k 1%
CHIP_3V3

HOST_RX_OUT
R8
10k 1%
HOST_RX_OUT

CHIP_3V3
HOST_3V3
R9
680R
LED_TX5_K

CHIP_RX_OUT
D5
KT-2012SGC
CHIP_RX_OUT

HOST_3V3
R10
680R
LED_RX5_K

HOST_RX_OUT
D6
KT-2012SGC
HOST_RX_OUT

05 / CHIP INTERFACE J4 = CHIP U13 (2x06), J3 = CHIP U14 (2x20), TP1–TP11 bottom pads

J4
CHIP_3V3
CHIP_5V
GND
GND
CHIP U13 SOCKET 2x06

J3
CHIP_TX_IN
CHIP_RX_OUT
CHIP U14 SOCKET 2x20

TP1
TP_GND
GND

TP2
TP_VIN_PROT
VIN_PROT

TP3
TP_BUCK_5V
BUCK_5V

TP4
TP_CHIP_5V
CHIP_5V

TP5
TP_CHIP_3V3
CHIP_3V3

TP6
TP_HOST_3V3
HOST_3V3

TP7
TP_HOST_TX_IN
HOST_TX_IN

TP8
TP_HOST_RX_OUT
HOST_RX_OUT

TP9
TP_CHIP_RX_OUT
CHIP_RX_OUT

TP10
TP_CHIP_TX_IN
CHIP_TX_IN

TP11
TP_GND
GND

06 / SHEET NOTES

PIN MAP: J1 (Gadgeteer U, 1.27 mm, 1 <-> +3.3 V, 2 <-> +5 V, 10 <-> GND). 9 <-> host TX (HOST_TX_IN). 5 <-> host RX (HOST_RX_OUT). 3, 6, 7, 8, 9 not connected (no-connect flags).

J4 = CHIP U13 2x06: 1 GND, 2 CHI->IN (CHIP_5V, the ONLY 5 V feed), 4 GND, 5 VCC->3V3 (OUTPUT used as the U2 supply), 3 VCC->5V is an OUTPUT: NEVER connect.

J3 = CHIP U14 2x20: 1 GND, 3 UART1-TX (CHIP_TX_IN), 5 UART1-RX (CHIP_RX_OUT); every other pin is mechanical retention (no-connect flags). Pin 7 FILL: never ground.

NEW ASSIGNMENT of J3/14: Look pins on the south row in the module top view) is DERIVED from drawings unpowered continuity gate U12 is mandatory before first power.

U2 host->CHIP: VCC = CHIP_3V3, OE = HOST_3V3. U3 CHIP->host: VCC = HOST_3V3, OE = CHIP_3V3. Each buffer is high-Z unless BOTH domains are powered: pull-ups return to their own domain.

LEDs: D5 TX5 and D6 RX5 (amber) light while the buffered line is LOW. D7 POWER 5V (green) means CHIP_5V is present, not READY. LED branches reference only their own rail.

POWER: J2 7–24 V DC SJ1/1. NO HOT-PLUG. D3/SJ2 are sacrificial (V4) shortly replace after a sustained fault. Common GND for host, external supply and CHIP.

TEST POINTS (bottom, observation only): TP1/TP11 GND, TP2 VIN_PROT, TP3 BUCK_5V, TP4 CHIP_5V, TP5 CHIP_3V3, TP6 HOST_3V3, TP7 HOST_TX_IN, TP8 HOST_RX_OUT, TP9 CHIP_RX_OUT, TP10 CHIP_TX_IN.

D2/D3 are unidirectional TVS (SMBJ24A / SMBJ5.0A) drawn with Device:D_Zener (K = pin 1, A = pin 2) because Device:D_TVS is bidirectional.

CERN-OHL-S-2.0 | KiCad only | black solder mask, white silkscreen | v01 STUDY: not fabrication-ready, not electrically qualified.

U1
VEXT_IN
VEXT_IN
P_chip_EN
P_chip_SCK
P_chip_MOSI
P_chip_MISO
P_chip_RTS
GND
P_chip_SCK
P_chip_SCK
P_chip_CS
VIN_FUSED
VIN_FUSED
P_chip_RTS
A
A
EN
SCK
MOSI_AUTOBOOT
MISO_CRTS
CS_NOT_USED
GND
SCK
MOSI_UNUSED
3.3V
POUT
CS
3.3V
GPIO_27
ESP32S3WROOM1
U1 ESP32-S3-WROOM-1-N16R8

RP1
VEXT_IN
P_chip_EN
4.2k 0.1%

RP2
P_chip_EN
P_chip_RTS
10k 0.1%

RP3
VEXT_IN
P_chip_SCK
100k 0.1%

RP4
P_chip_SCK
P_chip_MOSI
10k 0.1%

RP5
P_chip_SCK
P_chip_MISO
5.36k 0.1%

CP1
P_chip_SCK
P_chip_RTS
100nF 25V X7R

CP2
VEXT_IN
GND
100nF 50V X7R

CP3
VIN_FUSED
GND
1uF 50V X7R

RP6
P_chip_MOSI
VEXT_IN
10kx14bd1-7-7

RP7
P_chip_MISO
P_chip_27_R
10k 1%

SJP1
P_chip_27_R
P_chip_27_K
JUMPER

CP4
P_chip_27_K
P_chip_RTS
100nF 16V X7R

SJP2
P_chip_27
P_chip_27_K
JUMPER

SP2
P_chip_27
P_chip_27_K
1727-1170HR7

SP3
P_chip_EN_K
P_chip_EN_MOS
GND
1143180620

RP8
P_chip_EN_GATE
P_chip_EN_MOS
100k 0.1%

RP9
P_chip_EN_MOS
10k 0.1%

RP10
P_chip_MOSI
P_chip_EN_K
22k 0.25W

SP4
P_chip_EN_K
P_chip_EN_MOS
GND
BAT54WS-7-F

SJP3
P_chip_EN_R
P_chip_EN_K
JUMPER

RP11
P_chip_EN_MOS
GND
BAT54WS-7-F

SP5
P_chip_EN_K
P_chip_EN_L
1727-1170HR7

RP12
P_chip_RTC_VCC
P_chip_BAT
47k 1%

SP6
P_chip_RTC_FIX
GND
10kx14bd1-7-7

RP13
P_chip_RTC_VCC
P_chip_BAT
47k 1%

SP7
P_chip_RTC_FIX
P_chip_RTC_VCC
BAT54C-7-F

RP14
P_chip_RTC_VCC
P_chip_L1
10k 1%

SP8
P_chip_BU
VEXT_IN
P_chip_L1
MMBT3904-7-F

SP9
P_chip_BU
VEXT_IN
P_chip_L2
BAT54WS-7-F

RP15
P_chip_RTC_VCC
P_chip_L2
10k 1%

CP5
P_chip_L1
P_chip_BU
10nF 16V X7R HOHMSLAB

CP6
P_chip_L2
P_chip_BU
10nF 16V X7R HOHMSLAB

RP16
P_chip_RTC_VCC
P_chip_RTC_K
10k 1%

SJP3
P_chip_RTC_K
P_chip_RTC_K
JUMPER

DP8
P_chip_L1
P_chip_RTC_K
1727-1170HR7

SP10
P_chip_RTC_K
GND
BAT54WS-7-F

SP11
P_chip_EN_GATE
P_chip_EN_GATE
VEXT_IN
BSS84H-7-F

RP17
P_chip_EN_GATE
GND
100k 1%

SP12
P_chip_EN_GATE
P_chip_EN_GATE
BZT52C12S-7-F

CHIP v1.0 carrier. STUDY, not fabrication-ready.
Generated from design-contract.json by tools/create_schematic.py
SmoothWave / CERN-OHL-S-2.0
Sheet: /
File: chip-breakout.kicad_sch

Title: C.H.I.P. breakout board (v1.0 PCBA carrier)	
Size: A0	Date: 2026-11-01
KiCad E.D.A. 9.0.8	Rev: v1.0 Id: 1/1