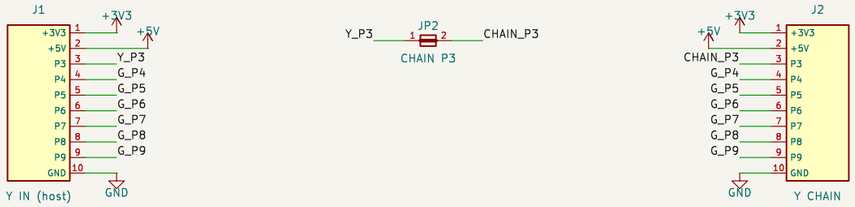
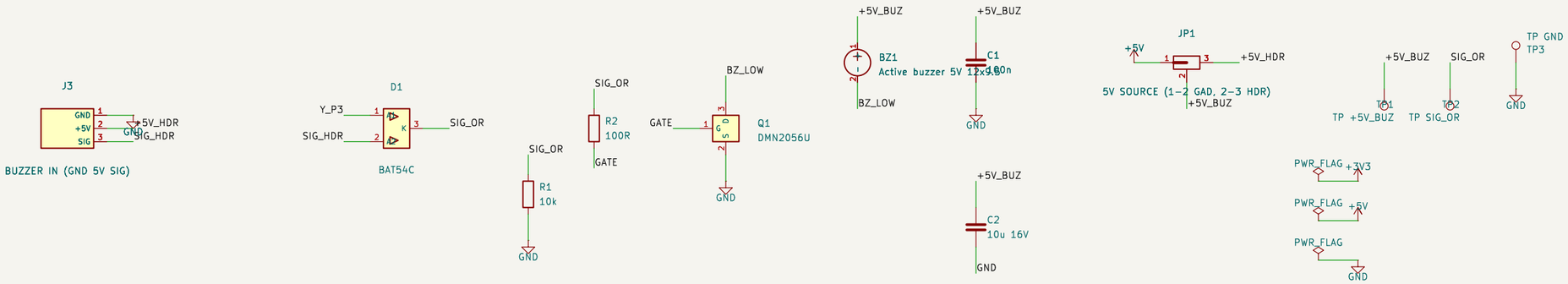
1 GADGETEER Y: HOST IN (J1) — CHAIN LINK JP2 (PIN 3) — CHAIN OUT (J2). PINS 4–9, +3V3, +5V, GND ARE DIRECT COPPER



Y_P3 = host side (the buzzer listens here, even with JP2 cut). CHAIN_P3 = downstream side. JP2 bridged at the factory.

G_P4..G_P9 pass J1 to J2 as direct copper: nothing on this board loads them, so there is nothing to isolate.

2 BUZZER CONTROL: INPUT OR (Y PIN 3 OR 3-PIN HEADER), LOW-SIDE DRIVER, 5V SOURCE LINK JP1, TEST PADS



PWR_FLAGs: +3V3, +5V and GND come from the host through J1; this board has no regulator.

NOTES

1. Pin map (Gadgeteer table, CLAUDE.md section 3): pin 1 +3V3, pin 2 +5V, pin 10 GND on every socket. The drive signal is the first signal pin, pin 3 (never pin 1).
2. SIG HIGH = BUZZ. Input OR: D1 BAT54C anodes = Y_P3 and SIG_HDR, cathode = SIG_OR. 10k R1 holds SIG_OR low (floating, reset, host unpowered = silent). R2 100R in the gate.
3. Driver: Q1 DMN2056U low-side switch. BZ1 CMI-1295-0585T is internally driven (30 mA typ at 5 V): DC level on = continuous tone; gate it with PWM or firmware for patterns.
4. 5V source JP1: pad 1 = Gadgeteer +5V (J1.2, factory bridged 1-2), pad 3 = 3-pin header +5V. Cut 1-2 and bridge 2-3 for header power. Cut both to mute / insert an ammeter. Never bridge all three.
5. 3-pin header J3 order is GND, +5V, SIGNAL (Smoothieboard single-output pinout). Use ONE input source: signals are OR-ed, 5 V rails are not merged unless JP1 is bridged 1-2-3.
6. Chain: J2 repeats J1 pin for pin; only pin 3 passes through the cuttable link JP2. No hot-plug claim. Power-off backfeed: BAT54C blocks one input from driving the other.
7. Study version v10: unqualified, not for fabrication. CERN-OHL-S-2.0, KiCad only.

STUDY: unqualified, not for fabrication
Active buzzer driven from Gadgeteer pin 3 or a 3-pin header
Smoothieware / CERN-OHL-S-2.0

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Title: Smoothie buzzer module

Size: A3	Date: 2026-10-11	**Rev: v10**
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