01 / ATX 24-PIN INPUT J1 (header viewed from the top, pin 1 west; north row 1–12, south row 13–24)



02 / FUSED OUTPUT CHANNELS: fuse -> TVS -> power LED -> connector (post-fuse side)



Channel order: F1/D1/R7/D4/J3 = +12V (XT60), F2/D2/R8/D5/J4 = +5V, F3/D3/R9/D6/J5 = +5VSB (always live).

UNQUALIFIED PROTOTYPE STUDY (hazard class high-current): UNSUITABLE FOR FABRICATION UNTIL HUMAN REVIEW. CAD design intent only.

Standard ATX12V v2.x / ATX v3.x 24-pin plug only. NOT ATX12VO. NOT 20-pin-only. NOT OEM (Dell/HP/Lenovo) pinouts. J1 numbering = plug numbering (Molex drawing check still open, U1).

J1 pins (viewing the header from the top, pin 1 west, north row 1–12, south row 13–24): 1,2:12,13 = +3V3 | 3,5,7,15,17,18,19,24 COM=GND | 4,6,21,22,23 = +5V | 8 PWR_OK | 9 +5VSB | 10,11 +12V | 14 -12V NC | 16 PS_ON# | 20 reserved NC.

Rails: +12V -> F1 (15 A 4TM blade, 10 A target) -> J3 XT60; +5V -> F2 (5 A, 3.75 A target) -> J4; +5VSB -> F3 (2 A, 1.5 A target) -> J5. ALWAYS LIVE while mains is present. -12V and +3.3V are not exposed.

Pre-fuse nets +12V_ATX, +5V_ATX, +5VSB_ATX carry no test pad. LED or tap (except R3 and R10 on +5VSB_ATX by design). TVS D1–D3 (SMBJ13A / SMBJ6.0A) sit on the load side of the fuses (exception E1: no TVS at the inlet).

PS_ON# is open-drain: Q1 (DMN2056U-7) pulls it low only when PSU_EN_IN (Gadgeteer X pin 3, active high) is high. R2 100k gate pull-down keeps the PSU OFF by default. J6 shunt = always on; external switch across J6 = manual.

PWR_OK (5 V, 1 kohm source) -> R4 1k -> PWR_OK_SENSE (R5 100k pull-down) -> U1 SN74LVC1G17 (VCC = host 3V3, 5.5 V tolerant input) -> R6 100R -> J_X pin 4, Q2 sinks the PWR_OK LED 27 from +5VSB via R10.

Gadgeteer X (CLAUDE.md Version 1A): pin 1 =3.3V, pin 2 =5V (host pass-through to J_C only, NEVER to an ATX rail), 3 PSU_EN_IN, 4 PWR_OK_OUT, 5–8 pass-through, 10 GND. J_C repeats J_X: JP3/JP4 OPEN. JP5–JP9 bridged.

Single ground net GND = ATX COM = host GND = output returns. Chassis/PE are not brought onto the board (exception E2). No hot-plug: unplug mains first, +5VSB is live on J1.

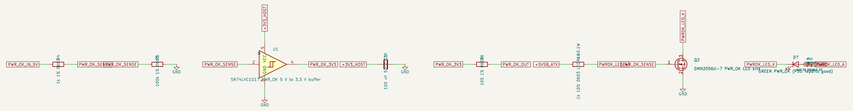
Test points TP1–TP12 are bottom-side observation pads (none on pre-fuse buses). TP4 +3V3 via R11 100R. F1_LINK (15 A mini blade fuse, Littelfuse 029701.5.WXNV) is a BOM-only line, not placed. H1–H4 M3 holes are board-only.

CERN-OHL-S-2.0 | KiCad only | black solder mask, white silkscreen | 2 layers 1 oz | Smoothieware extension boards.

03 / PS_ON# CONTROL (open drain, default OFF) AND MANUAL HEADER J6



04 / PWR_OK PATH (5 V PSU to 3.3 V host) AND PWR_OK LED



05 / GADGETEER X HOST SOCKET J_X, CHAIN SOCKET J_C, CHAIN JUMPERS JP3–JP9 (pad 1 = host side, pad 2 = chain side)

06 / TEST POINTS (bottom side) AND +3V3 TEST RESISTOR



Power flags: +12V_ATX +5V_ATX +5VSB_ATX +3V3_ATX +3V3_HOST +5V_HOST GND



ATX 24-pin to fused XT60/terminals, PS_ON# open drain, PWR_OK to host, Gadgeteer X + chain, UNQ
Retained v01 schematic plus v02 exact footprint aliases; nodes unchanged
Smoothieware / CERN-OHL-S-2.0
Sheet: /
File: atx-connector-board.kicad_sch

Title: Smoothie ATX connector board

Size: A2	Date: 2026-10-01	**Rev: v02**
KiCad E.D.A. 9.0.8		Id: 1/1